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10EC63

Sixth Semester B.E. Degree Examination, June/July 2019
Microelectronic Circuits

Time: 3 hrs. Max. Marks:100

Note: ***Answer any THREE full questions from Part-A and any TWO full questions from Part-B.***

PART – A

1 a. With a diagram and characteristic curves, derive relationship between $i_D - V_{DS}$ and discuss the characteristics for an enhancement NMOS transistor. **(10 Marks)**

b. Analyze the circuit shown in Fig.Q.1(b) to determine the voltages at all nodes and the currents through all branches. Let $V_t = 1V$, $K_n^1\left(\frac{W}{L}\right) = 1mA/V^2$ and assume $\lambda = 0$. **(05 Marks)**

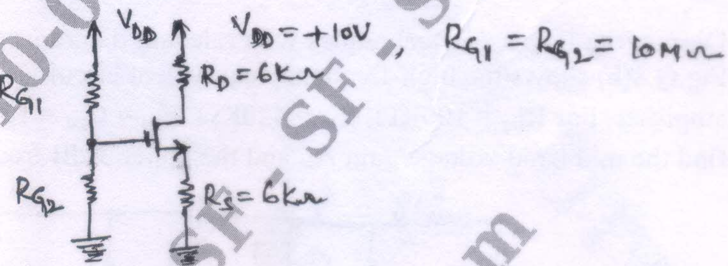

Fig.Q.1(b)

c. Consider a process technology for which $L_{min} = 0.4\mu m$, $t_{ox} = 8nm$, $\mu_n = 450\ cm^2/v.s$ and $V_t = 0.7v$,

i) Find C_{ox} and k_n^1

ii) For a MOSFET with W/L = 8μm/0.8μm, calculate the values of V_{GS} and V_{DSmin} needed to operate the transistor in the saturation region with a dc current $I_D = 100\mu A$.

iii) For the device in (ii), find the value of V_{GS} required to cause the device to operate as a 1000Ω resistor for very small V_{DS}. **(05 Marks)**

2 a. Explain the following with the help of a diagram and waveforms:

i) DC bias point

ii) Signal current in the drain terminal

iii) Voltage gain. Derive appropriate equations. **(10 Marks)**

b. For the devices in the circuit of Fig.Q.2(b), $|V_t| = 1v$, $\lambda = 0$, $\gamma = 0$, $\mu_n C_{ox} = 50\mu A/v^2$, L = 1μm, w = 10μm, find V_2 and I_2. How do these values change if Q_3 and Q_4 are made to have W = 100μm? **(05 Marks)**

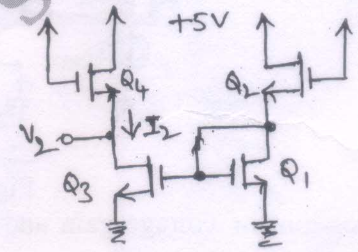

Fig.Q.2(b)

c. Using the feedback bias arrangement shown in Fig.Q.2(c) with a, 9V supply and NMOS device for which $V_t = 1v$, $K_n^1\left(\frac{W}{L}\right) = 0.4mA/v^2$, find R_D to establish a drain current of 0.2mA. If resistor values are limited to those on the 5% resistor scale, what value would you choose? What values of current and V_D result? **(05 Marks)**

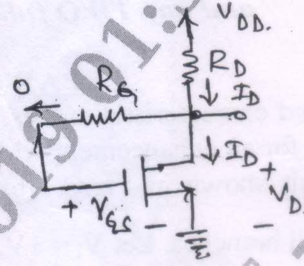

Fig.Q.2(c)

3 a. Discuss the IC biasing techniques with relevant diagrams and expressions. **(10 Marks)**

b. Fig.Q.3(b) shows the high-frequency equivalent circuit of a common source MOSFET amplifier. For $R_{sig} = 100K\Omega$, $R_{in} = 420K\Omega$, $C_{gs} = C_{gd} = 1pf$, $g_m = 4mA/v$, $R_L^1 = 3.33K\Omega$, find the mid band voltage gain A_m and the upper 3-dB frequency, f_H. **(06 Marks)**

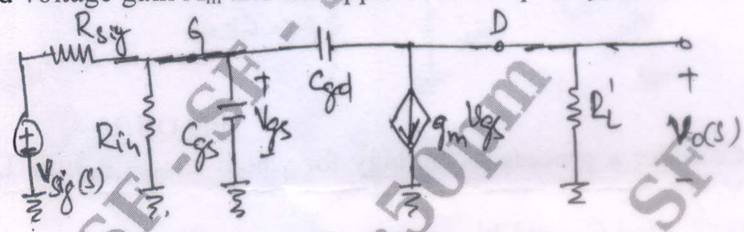

Fig.Q.3(b)

c. With an equivalent circuit discuss Miller's theorem. **(04 Marks)**

4 a. A CMOS common-source amplifier shown in Fig.Q.4(a) has W/L = 7.2 μm/0.36μm for all transistors, $\mu_n C_{ox} = 387\ \mu A/v^2$, $\mu_p C_{ox} = 86\ \mu A/v^2$, $I_{REF} = 100\mu A$, $V_{An}^1 = 5v/\mu m$, $|V_{AP}^1| = 6V/\mu m$. For Q_1, $C_{gs} = 20fF$, $C_{gd} = 5fF$, $C_L = 25fF$, $R_{sig} = 10K\Omega$. Assume C_L includes all capacitances of Q_2 at the output mode. Find f_H using Miller equivalence and the open circuit time constants. Also determine the exact values of fp_1, fp_2 and fz and hence provide another estimate for f_H. **(09 Marks)**

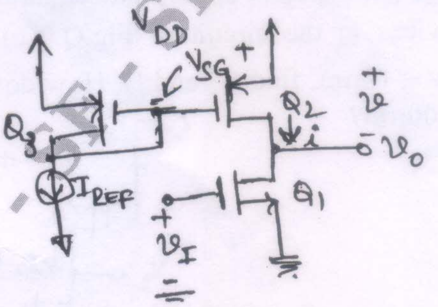

Fig.Q.4(a)

b. Derive an expression for voltage gain and high frequency response of CG amplifier with active loads. **(08 Marks)**

c. Discuss the bipolar mirror with base-current compensation. **(03 Marks)**

5 a. With diagram, derive an expression for input offset voltage of the differential pair. **(07 Marks)**

b. Consider an active-loaded MOS differential amplifier shown in Fig.Q.5(b). Assume for all transistors, $\frac{W}{L} = 8.2\mu m / 0.36\mu m$, $C_{gs} = 20fF$, $C_{gd} = 5fF$, $C_{db} = 5$ fF. Let $\mu_n C_{ox} = 387\ \mu A/v^2$, $\mu_p C_{ox} = 86\ \mu A/v^2$, $V^1_{An} = 5v/\mu m$, $|V^1_{Ap}| = 6v/\mu m$. Bias current I = 0.2mA, $R_{ss} = 25K\Omega$, $C_{ss} = 0.2PF$ and the capacitance at output node $C_x = 25fF$. Determine the low-frequency values of A_d, A_{cm} and CMRR. Also find the poles and zero of A_d and the dominant pole of CMRR. **(09 Marks)**

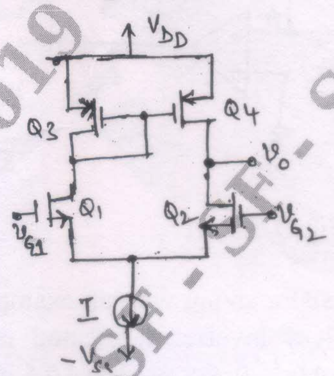

Fig.Q.5(b)

c. With a diagram, explain the two-stage CMOS OPAmp. **(04 Marks)**

PART – B

6 a. Explain the properties of negative feedback. **(08 Marks)**

b. For the OpAmp circuit shown in Fig.Q.6(b), $\mu = 10^4$, $R_{id} = 100K\Omega$, $r_0 = 1k\Omega$, $R_L = 2K\Omega$, $R_1 = 1K\Omega$, $R_2 = 1M\Omega$ and $R_s = 10K\Omega$. Find the values for A, β, the closed – loop gain (v_o/v_s), input resistance (R_{in}) and the output resistance (R_{out}). **(07 Marks)**

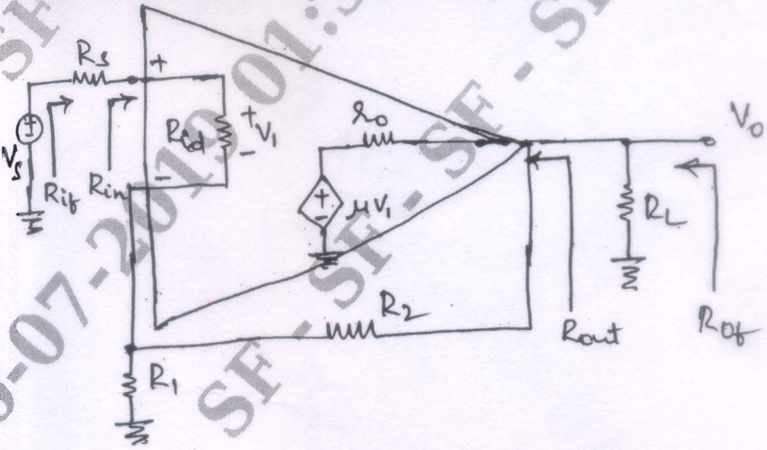

Fig.Q.6(b)

c. Discuss the effect of feedback on the amplifier with two-pole response. **(05 Marks)**

7 a. Discuss and derive an expression for output voltage of antilogarithmic amplifiers. **(05 Marks)**

b. With a diagram, derive an expression for common mode gain of single Op-Amp difference amplifier. **(07 Marks)**

c. Assuming OpAmp to be ideal, derive an expression for closed-loop gain (v_O/v_I) of the circuit shown in Fig.Q.7(c)(i). Using this circuit design an inverting amplifier with a gain of 100, input resistance of 1MΩ. For practical reasons, not to use the resistors greater than 1MΩ. Compare your design with the circuit shown in Fig.Q.7(c)(ii). **(08 Marks)**

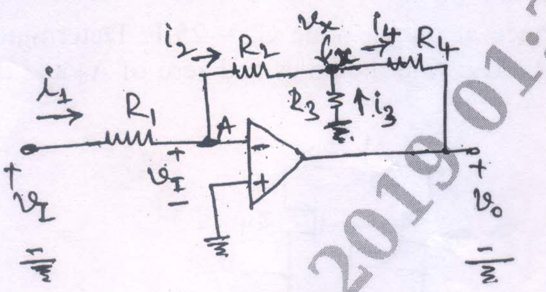

Fig.Q.7(c)(i)

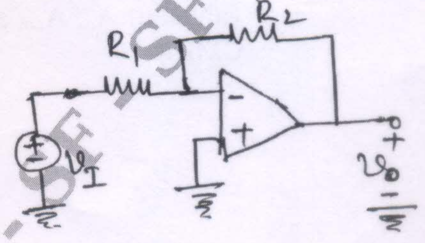

Fig.Q.7(c)(ii)

8 a. Explain the transistor sizing with an example of 4 input NAND gate. **(06 Marks)**

b. Consider a CMOS inverter fabricated in a 0.25μm process for which C_{ox} = 6fF/μm^2, μn C_{ox} = 115μA/v^2, $\mu_p C_{ox}$ = 30μA/v^2, V_{tn} = -V_{tp} = 0.4V, V_{DD} = 2.5V. W/L ratio for Q_N = 0.375 μm/0.25μm and for Q_P = 1.125μm/0.25μm, C_{gs} = C_{gd} = 0.3fF/μm of gate width, C_{dbh} = 1fF, C_{dbp} = 1fF and C_w = 0.2fF. Find t_{PHL}, t_{PLH} and t_P. **(07 Marks)**

c. Explain the parameters used to characterize the operation and performance of logic family. **(07 Marks)**

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